Amendment to the Drawings:

Attached as an Appendix to this Amendment is a new drawing sheet adding new FIG. 16.

REMARKS

This Amendment, which is timely with the accompanying Petition for Extension of Time, is submitted in response to the Office Action mailed November 16, 2005. In the Office Action all of the pending claims, namely claims 17 – 24, 26 – 34, and 36 – 44 were rejected as obvious in view of various prior art references, discussed below. Claims 28 and 44 were also rejected under 35 U.S.C. § 112, first paragraph, and the drawings were objected to under 37 C.F.R. § 1.83(a). By this amendment, claims 17, 40 and 44 have been amended. Thus, claims 17 – 24, 26 – 34 and 36 – 44 remain pending. Reconsideration and reexamination are respectfully requested.

Drawing Objections

The drawings were objected to as failing to show every feature of the invention specified in the claims. The applicant is very concerned about the examiner's piecemeal approach to examination, where new drawing objections are raised with each Office Action. The examiner is reminded of 37 C.F.R. § 1.104 which requires that the examiner's Office Action be "complete" and MPEP § 707.07(g) which requires avoidance of piecemeal examination.

The drawing objections are ***traversed*** because all of the features of claims ***are*** shown in the drawings, which is all that is required. There is ***NO*** legal requirement in the statute, the rules or the MPEP that all of the features recited in a claim be shown in a ***single*** drawing and frequently it would be impossible to do so. It is extremely commonplace for different aspects of an invention to shown in different drawing figures. Moreover, the specification of the present application specifically describes the fact that the features depicted in the drawings can be combined in different ways.

Nonetheless, applicant has submitted herewith a new drawing sheet comprising a new FIG. 16 which depicts an embodiment containing all the features recited in claims 28, 30 – 33 and 44. The embodiment of FIG. 16 is substantially the same as the embodiment of FIG. 9, except that components 20 are lodged in cavities in core 12. FIG. 16 is thus supported by original FIG. 9, and the related discussion thereof, and by paragraph [0028] of the published application.

Traversal of Section 112 Rejections

Claims 28 and 44 were rejected under 35 U.S.C. § 112, first paragraph, as failing to meet the written description requirement. Applicant respectfully ***traverses*** these rejections. Claim 28, which is dependent on original claim 24, specifies that the second electronic component of claim 24 has a conductive pad that contacts the "second metallic layer." As per claim 18, the "second metallic layer" is disposed on the "second substrate surface." Thus, for example, the "second metallic layer" of the illustrated figures is patterned layer 16. Paragraph [0028] of the published application (*i.e.*, the application as filed), reads in pertinent part:

> In another embodiment of the present invention ***one or both of the substrate surfaces 12a and 12b may have a cavity*** generally illustrated as 24 in FIG. 12. The cavity 24 may be formed by any suitable means, such as by milling, cutting or drilling. The prefabricated, integrated circuit component 20 (e.g., resistors, capacitors, inductors, etc.) may be conveniently disposed in the cavity 24, as shown in FIG. 13. (Emphasis added.)

Moreover, as shown in FIG. 13, when a component is embedded in a cavity in substrate 12, it may have contact pads 26, which contact the metal layer overlying the substrate surface. Thus, in FIG. 13, pads 26 are shown contacting patterned metal layer 14. This is also illustrated in new FIG. 16.

Claim 44 specifies a "third dielectric layer" on the second side of the core substrate. The "third dielectric layer" is shown, for example, as layer 32 in FIG. 9. As indicated, layer 32 is disposed on the second side (side 12b – see FIGS. 1 – 6) of core substrate 12, and has a patterned metallic layer 42 formed thereon. As indicated above, the specification as originally filed expressly states that component 20 can either be on substrate 12, or within a cavity formed in substrate 12.

Claim Amendments

Independent claims 17, 40 and 44 have been amended to recite that there is a via ***at one location*** which extends through the first and second dielectric layers. This is shown, for example, in FIG. 9 of the application as originally filed, and in new FIG. 16, as vias 70, and is described in paragraph [0032] of the published application (*i.e.*, the application as originally filed).

Traversal Of Claim Rejections

One of the primary references cited against all of the claims is Ma et al., U.S. Pat. No. 6,154,366 ("Ma"). Ma does not show or suggest, alone or in combination with any of the other references of record, a via ***at one location*** that extends through first ***and*** second dielectric layers and which are coupled to an integrated electronic component positioned in a cavity of a polymeric substrate. The claims, as amended, require the use of a single via that is formed through multiple dielectric layers. In contrast, Ma shows multiple interconnected and staggered vias.

Moreover, Ma merely shows an IC chip which is mounted on a flexible wiring interconnect, referred to in the patent as a "flex component." The chip is then encapsulated with an encapsulant, and additional wiring layers may be added onto the flex component. Ma is principally directed to the use of moisture barriers surrounding the chip. Ma does not show a cavity formed in a core substrate in which a prefabricated component is mounted. In this regard, surrounding a component that has already be connected to a substrate with an encapsulating material is much different than securing a prefabricated component in a cavity that has been pre-formed in a substrate.

The second primary reference cited by the examiner is Miura et al., U.S. Pat. No. 5,565,706, ("Miura"). All of the independent claims specify that the core substrate is "polymeric." ALL of the embodiments discussed in Miura use ceramic or silicon core substrates. This is true notwithstanding the fact that the patent discloses the use of polymers for other purposes. It is further noted that the one embodiment which uses a silicon core substrate does NOT form a cavity in the silicon substrate – in fact FIG. 11 does not show any devices mounted on the silicon, presumably, as stated in the patent, because silicon is susceptible to warping.

Applicant respectfully submits that it would not have been obvious to substitute the polymeric core substrate of the present invention for Miura's ceramic core substrates. Miura carefully and consistently differentiates ceramic substrates from polymeric substrates. Thus, for example, it contains an extended discussion under the heading, "Description of the Related Art," differentiating ceramic wiring boards and polymeric wiring boards. It is clear from this discussion that the two are <u>not</u> considered interchangeable. One important difference between

ceramic and polymeric substrates is their respective thickness. The ceramic substrates disclosed in Miura are 0.8 mm (800 microns) thick, whereas the polymeric layers disclosed in the patent are 40 microns thick – *i.e.*, 5% of the ceramic substrate thickness. In addition, ceramic processing technology is quite different than polymeric processing technology. Because of the significant size and processing differences between these two technologies, persons of skill in the art do not view the two as interchangeable. Thus, there is no reason shown why someone skilled in the art would be motivated to replace the ceramic substrate of Miura with a polymeric substrate. The examiner merely asserts that it would be obvious to substitute the resin core substrate of Saito for the ceramic core substrate of Miura. This mere assertion is insufficient, the examiner is legally required to show some suggestion or other motivation for making the substitution.

Claims 36, 37 and 40 – 43 all required that prefabricated capacitors be incorporated into cavities formed in polymeric core substrates. None of the prior art of record relied upon by the examiner shows capacitors secured in cavities in polymeric substrates. Claims 37 and 42 further specify that the capacitors comprise a petrovskite capacitance material. The examiner has failed to show any motivation for combining the teachings of either of the primary references with Miyazawa.

Conclusion

In view of the amendments and remarks made above, applicant respectfully submits that the application is in condition for allowance and action to that end is respectfully solicited. The examiner is invited to telephone the undersigned at the number listed below if it is believed that a telephone interview would advance the prosecution of this matter.

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Respectfully submitted,

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